REMARKS

In accordance with the foregoing, claim 35 has been amended. Claims 12, 14-16, 22, and 24-38 are pending, with claims 12 and 22 being independent. No new matter is presented in this Amendment.

Claim Amendments

Claim 35 has been amended to insert a colon at the end of line 1.

Request that Examiner Consult with SPE about Extended Prosecution of Present Application

The present application has been pending since February 8, 2002, which is more than six years, and the Office Action of January 16, 2008, is the 13th Office Action that has been issued in the present application, with only two Requests for Continued Examination (RCEs) having been filed, on June 16, 2004, and October 31, 2007. The Examiner's attention is directed to MPEP 702, which provides as follows (emphasis added):

> **707.02 Applications Up for Third Action and 5-Year Applications**
>
> The supervisory patent examiners should impress their assistants with the fact that the shortest path to the final disposition of an application is by finding the best references on the first search and carefully applying them.
>
> The supervisory patent examiners are expected to personally check on the pendency of every application which is up for the third or subsequent Office action with a view to finally concluding its prosecution.
>
> Any application that has been pending five years should be carefully studied by the supervisory patent examiner and every effort should be made to terminate its prosecution. In order to accomplish this result, the application is to be considered "special" by the examiner.

In light of this, it is respectfully requested that the Examiner consult with his SPE about the extended prosecution of the present application.

Incorrect Statement in "Response to Arguments" Section of Office Action of January 16, 2008

In the "Response to Arguments" section on page 11 of the Office Action of January 16, 2008, the Examiner states as follows:

> Applicant's arguments filed 10/31/2007 have been fully considered but they are not persuasive. See Office Action mailed 11/7/2007.

However, it is submitted that this statement cannot be correct because the Examiner did not know that the Amendment Accompanying Request for Continued Examination (RCE) of October 31, 2007, had been filed when he issued the Final Office Action of November 7, 2007, such that the Examiner did not consider the arguments in the Amendment Accompanying Request for Continued Examination (RCE) of October 31, 2007, in the Final Office Action of November 7, 2007.

Furthermore, it appears from the record that the arguments in the Amendment Accompanying Request for Continued Examination (RCE) of October 31, 2007, were in fact persuasive because in the Office Action of January 16, 2008, the Examiner has withdrawn all of the previous rejections of the claims and has set forth new grounds of rejection of the claims, some of which rely on the Ohtani reference, which was newly cited by the Examiner in the Office Action of January 16, 2008. However, some of the rejections in the Office Action of January 16, 2008, are similar to some of the rejections in the Final Office Action of November 7, 2007, in that in the Office Action of January 16, 2008, the Examiner has relied on U.S. counterparts of Japanese references relied on by the Examiner in the Final Office Action of November 7, 2007.

Claim Rejections Under 35 USC 103

In explaining the five rejections under 35 USC 103(a), the Examiner relies on specific figures and specific portions of Takemura, Yamazaki '648, Ohtani, and Yamazaki '502. Should the Examiner change his position and rely on different figures and/or portions of these references and/or different combinations of these references in response to the following arguments pointing out deficiencies in the rejections, it is submitted that such a change in position will constitute a new ground of rejection, such that the Examiner will not be able to make the next Office Action final since the claims have not been amended in the present Amendment, except to insert a colon at the end of the first line of claim 35.

Rejections 1 and 4

Claims 12, 14-16, 26, and 28-31 (rejection 1) and claims 22, 24, 27, and 32-34 (rejection 4) have been rejected under 35 USC 103(a) as being unpatentable over Takemura et al. (Takemura) (U.S. Patent No. 5,962,897) in view of Yamazaki et al. '648 (Yamazaki '648) (U.S. Patent No. 6,617,648). These rejections are respectfully traversed.

Claim 12

The Examiner considers FIGS. 5A-5D and 6A-6D of Takemura to disclose all of the features of independent claim 12 except the "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers," which the Examiner considers to be taught in FIGS. 6A-6E of Yamazaki '648.

However, it is submitted that Takemura does not disclose or suggest "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer" as recited in claim 12 as alleged by the Examiner because in FIGS. 5A-5D and 6A-6D of Takemura relied on by the Examiner, the spacers 22 are not formed on sidewall portions of the gate electrode 15, but are formed on sidewall portions of the capping layer 16, and in FIGS. 6A-6D of Takemura relied on by the Examiner, the spacers 22 are not formed over the first insulating layer 14, but are formed over the semiconductor layer 13.

Furthermore, although the Examiner is of the opinion that it would have been obvious to provide the "low-density source and drain regions . . . under said spacers" taught in FIGS. 6A-6E Yamazaki '648 in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura "to minimize kink effect," Takemura does not mention the kink effect, and Yamazaki '648 only contains cursory references to the kink effect in column 2, lines 7 and 14, in the "Summary of the Invention" section, and it is not seen where Yamazaki '648 discloses that providing "low-density source and drain regions . . . under said spacers" would minimize the kink effect as alleged by the Examiner. Accordingly, it is submitted that there is no basis in Takemura and Yamazaki '648 for the

motivation relied on by the Examiner to combine Takemura and Yamazaki '648 as proposed by the Examiner, such that the Examiner has not established a *prima facie* case of obviousness with respect to claim 12. Nor has the Examiner identified any basis for the motivation elsewhere in the prior art.

Claim 22

The Examiner considers FIGS. 5A-5D and 6A-6D of Takemura to disclose all of the features of independent claim 22 except "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at entireties of off-set regions of said semiconductor layer entirely under said spacers, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers," which the Examiner considers to be taught in FIGS. 6A-6E of Yamazaki '648, and "a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes" and "a pixel electrode formed on the planarization layer, the pixel electrode contacting the portion of the one of the source and drain electrodes through the opening portion," which the Examiner considers to be taught in FIG. 5C of Yamazaki '648.

However, it is submitted that Takemura does not disclose or suggest "spacers formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer" as recited in claim 22 as alleged by the Examiner for at least the same reasons discussed above that Takemura does not disclose or suggest the similar feature of claim 12.

Furthermore, it is submitted that it would not have been obvious to provide the "low-density source and drain regions . . . under said spacers" allegedly taught in FIGS. 6A-6E of Yamazaki '648 in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura as proposed by the Examiner for at least the same reasons discussed above in connection with the similar feature of claim 12.

Furthermore, the Examiner has not clearly articulated any reasons why it would have been obvious for one of ordinary skill in the art to use the planarization layer 349 and the pixel electrode 350 in FIG. 5C of Yamazaki '648 in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura as required by MPEP 2143, such that the Examiner has not established a *prima facie* case of obviousness with respect to claim 22.

Furthermore, it is submitted that Takemura and Yamazaki '648 do not disclose or suggest "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at entireties of off-set regions of said semiconductor layer entirely under said spacers, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers" as recited in claim 22 because the ends of the source and drain regions 17 and 19 in FIGS. 5A-5D and 6A-6D of Takemura adjoining the channel forming region 18 are not formed entirely under the spacers 22 because the annealing process that is performed between FIGS. 5A and 5B and between FIGS. 6A and 6B as described in column 16, lines 40-56, of Takemura heats up the crystalline silicon film 13 and causes the previously implanted phosphorus to diffuse into the channel forming region 18. See column 16, lines 51-56, of Takemura, which reads as follows:

> Since phosphorus diffuses into the channel forming region to some extent during the annealing process, the boundary between the channel forming region 18 and the source/drain regions 17 and 19 is shifted nearer to the channel forming region 18 from the outer side of the oxide layer 16.

It is submitted that this same situation is present in FIGS. 6A-6E of Yamazaki '648, even though this is not shown in FIGS. 6A-6E of Yamazaki '648, because the heat treatment that is performed in FIG. 6D of Yamazaki '648 as described in column 13, lines 20-33, of Yamazaki '648 would cause the phosphorus that was implanted in FIG. 6B of Yamazaki '648 as described in column 13, lines 6-8, of Yamazaki '648 to diffuse into the channel forming region 612 for the reasons discussed in the above passage of Takemura. Accordingly, it is submitted that the low-density source and drain regions 611 in FIGS. 6A-6E of Yamazaki '648 are not actually formed entirely under the spacers 608.

Claim 28

It is submitted that Takemura and Yamazaki '648 do not disclose or suggest the feature "wherein said low-density source and drain regions having a same conductivity as said high-density source and drain regions are formed at entireties of regions of said semiconductor layer entirely under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers" recited in dependent claim 28 for at least the same reasons

discussed above that Takemura and Yamazaki '648 do not disclose or suggest the similar feature of claim 22.

Claims 31 and 34

It is submitted that Takemura and Yamazaki '648 do not disclose or suggest the feature "wherein the source and drain electrodes do not contact the spacers" recited in dependent claims 31 and 34.

As apparently recognized by the Examiner, Takemura does not disclose or suggest this feature of claims 31 and 34 because in FIGS. 5A-5D and 6A-6D of Takemura relied on by the Examiner, the source and drain electrodes 29 and 30 contact the spacers 22. However, the Examiner considers this feature to be taught in FIG. 6E of Yamazaki '648, stating as follows:

> Re claim 31, Yamazaki '892 [*sic*; presumably '648] discloses source and drain electrodes (614, 615) that do not contact a capping layer 605; and wherein the source and drain electrodes do not contact the spacers 608.

However, the Examiner has not clearly articulated any reasons why it would have been obvious for one of ordinary skill in the art to use the source and drain electrodes 614 and 615 in FIGS. 6E of Yamazaki '648 in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura as required by MPEP 2143, such that the Examiner has not established a *prima facie* case of obviousness with respect to claims 31 and 34.

Furthermore, it is submitted that the Examiner's apparent proposal to use the source and drain electrodes 614 and 615 in FIG. 6E of Yamazaki '648 in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura is inconsistent with the feature "source and drain electrodes which respectively contact said high-density source and drain regions without contact holes" recited in claims 12 and 22 from which claims 31 and 34 depend because the source and drain electrodes 614 and 615 in FIG. 6E of Yamazaki '648 contact the source and drain regions 609 and 610 through contact holes.

Furthermore, it is submitted that column 17, line 61, through column 18, line 6, of Takemura specifically teaches away from the Examiner's apparent proposal to use the source and drain electrodes 614 and 615 in FIG. 6E of Yamazaki '648 in the thin film transistors in FIGS.

5A-5D and 6A-6D of Takemura. Specifically, column 17, line 61, through column 18, line 6, of Takemura, states as follows in discussing FIGS. 5A-5D of Takemura (emphasis added):

> The NTFT thus, obtained comprises a triangular silicon oxide 22 to establish a contact portion between the source/drain regions and the contact in a so-called self-aligned manner. Moreover, the position of the contact portion can be set irrespective of the shrinking of the glass substrate 11. Furthermore, the contact portion can be set very near to the channel forming region. More advantageously, the sheet resistance of the source/drain regions is reduced by incorporating the silicide layer 28. In this manner, a high-performance TFT can be obtained. In addition, since the step of perforating the gate insulator film for establishing the source/drain contacts can be eliminated, problems associated with this step can be circumvented.

See the similar passage in column 18, lines 51-67, discussing FIGS. 6A-6D of Takemura. See also column 25, lines 33-45, of Takemura, which reads as follows (emphasis added):

> As described in the foregoing, the present invention is of great use in fabricating TFTs with improved characteristics and yet, with increased product yield.
>
> In addition to above, the position of the contact in the source/drain regions can be automatically set by providing the insulator in contact with the gate contact in a self aligned manner. Further advantage is that a structure without making special consideration of the sheet resistance of the source/drain regions can be obtained. In particular, devices free of mask matching and problems associated with the formation of contact holes can be obtained while setting the distance between the contact portion and the channel forming region in a self aligned manner.

Thus, by forming the contacts 29 and 30 in FIGS. 5D and 6D of Takemura so that they contact the spacers 22, the positions of the contacts 29 and 30 can be automatically set very near to the channel forming region 18, and the problems associated with the formation of contact holes, such as the contact holes in FIG. 6E of Yamazaki '648, can be avoided.

Conclusion—Rejections 1 and 4

For at least the foregoing reasons, it is respectfully requested that the rejection of claims 12, 14-16, 26, and 28-31 (rejection 1) and claims 22, 24, 27, and 32-34 (rejection 4), i.e., claims

12, 28, and 31 discussed above and claims 14-16, 26, 29, and 30 depending from claim 12, and claims 22 and 34 discussed above and claims 24, 27, 32, and 33 depending from claim 22) under 35 USC 103(a) as being unpatentable over Takemura in view of Yamazaki '648 be withdrawn.

Rejections 2 and 3

Claims 12, 26, 28-31, 35, and 36 (rejection 2) and claims 22, 24, 27, 32-34, 37, and 38 (rejection 3) have been rejected under 35 USC 103(a) as being unpatentable over Takemura in view of Ohtani et al. (Ohtani) (U.S. Patent Application Publication No. 2007/0210451). These rejections are respectfully traversed.

In explaining the rejection of claims 22, 24, 27, 32-34, 37, and 38 under 35 USC 103(a) as being unpatentable over Takemura in view of Ohtani on pages 6-8 of the Office Action of January 16, 2008, the Examiner refers to claim 36 on page 8 of the Office Action of January 16, 2008. It is presumed that the Examiner intended to refer to claim 38.

Claim 12

The Examiner considers FIGS. 5A-5D and 6A-6D of Takemura to disclose all of the features of independent claim 12 except the "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers," which the Examiner considers to be taught in FIGS. 4(A)-4(F) of Ohtani.

However, it is submitted that Takemura does not disclose or suggest "spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer" as recited in claim 12 as alleged by the Examiner because in FIGS. 5A-5D and 6A-6D of Takemura relied on by the Examiner, the spacers 22 are not formed on sidewall portions of the gate electrode 15, but are formed on sidewall portions of the capping layer 16, and in FIGS. 6A-6D of Takemura relied on by the Examiner, the spacers 22 are not formed over the first insulating layer 14, but are formed over the semiconductor layer 13.

Furthermore, although the Examiner is of the opinion that it would have been obvious to provide the "low-density source and drain regions . . . under said spacers" taught in FIGS. 4(A)-4(F) of Ohtani in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura "to minimize kink effect," Takemura and Ohtani do not mention the kink effect. Accordingly, it is submitted that there is no basis in Takemura and Ohtani for the motivation relied on by the Examiner to combine Takemura and Ohtani as proposed by the Examiner, such that the Examiner has not established a *prima facie* case of obviousness with respect to claim 12. Nor has the Examiner identified any basis for the motivation elsewhere in the prior art.

Claim 22

The Examiner considers FIGS. 5A-5D and 6A-6D of Takemura to disclose all of the features of independent claim 22 except "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at entireties of off-set regions of said semiconductor layer entirely under said spacers, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers," and "a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes," and "a pixel electrode formed on the planarization layer, the pixel electrode contacting the portion of the one of the source and drain electrodes through the opening portion," which the Examiner considers to be taught in FIGS. 4(A)-4(F) of Ohtani.

However, it is submitted that Takemura does not disclose or suggest "spacers formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer" as recited in claim 22 as alleged by the Examiner for at least the same reasons discussed above that Takemura does not disclose or suggest the similar feature of claim 12.

Furthermore, it is submitted that it would not have been obvious to provide the "low-density source and drain regions . . . under said spacers" allegedly taught in FIGS. 4(A)-4(F) of Ohtani in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura as proposed by the Examiner for at least the same reasons discussed above in connection with the similar feature of claim 12.

Although the Examiner refers to "a planarization layer 73" in FIGS. 4(A)-4(F) of Ohtani in explaining the rejection, it is noted that element 73 is a silicide layer in FIG. 4(D) of Ohtani. It is

presumed that the Examiner is actually referring to the interlayer dielectric 78 shown in FIG. 4(F) of Ohtani and described in paragraph [0067], line 1, of Ohtani. However, the left side of the "8" in reference number 78 is light, making "78" look like "73."

In any event, it is submitted that the interlayer dielectric 78 in FIG. 4(F) of Ohtani is not "a planarization layer" as recited in claim 22 as alleged by the Examiner because it does not form a planar surface. Furthermore, according to paragraph [0067], line 4, of Ohtani, is a conductive interconnect, not "a pixel electrode" as recited in claim 22 as alleged by the Examiner. The word "pixel" only appears in Ohtani in paragraph [0040], line 7, in the description of FIGS. 1(A)-1(F), and in paragraph [0056], line 7, in the description of FIGS. 3(A)-3(F).

Furthermore, the Examiner has not clearly articulated any reasons why it would have been obvious for one of ordinary skill in the art to use the alleged planarization layer 78 and the alleged pixel electrode 79 in FIG. 4(F) of Ohtani in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura as required by MPEP 2143, such that the Examiner has not established a *prima facie* case of obviousness with respect to claim 22.

Furthermore, it is submitted that Takemura and Ohtani do not disclose or suggest "low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at entireties of off-set regions of said semiconductor layer entirely under said spacers, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers" as recited in claim 22 because the ends of the source and drain regions 17 and 19 in FIGS. 5A-5D and 6A-6D of Takemura adjoining the channel forming region 18 are not formed entirely under the spacers 22 because the annealing process that is performed between FIGS. 5A and 5B and between FIGS. 6A and 6B as described in column 16, lines 40-56, of Takemura heats up the crystalline silicon film 13 and causes the previously implanted phosphorus to diffuse into the channel forming region 18. See column 16, lines 51-56, of Takemura, which reads as follows:

> Since phosphorus diffuses into the channel forming region to some extent during the annealing process, the boundary between the channel forming region 18 and the source/drain regions 17 and 19 is shifted nearer to the channel forming region 18 from the outer side of the oxide layer 16.

It is submitted that this same situation is present in FIGS. 4(A)-4(F) of Ohtani as can be seen in FIG. 7 of Ohtani, which is an enlarged cross section of 4(E) of Ohtani as descried in

paragraphs [0036] and [0068] of Ohtani. This is presumably the case because the thermal annealing that is performed in FIG. 4(C) of Ohtani as described in paragraph [0066] of Ohtani causes the phosphorus that was implanted in FIG. 4(A) of Ohtani as described in paragraph [0063] of Ohtani to diffuse into the channel region (corresponding to reference number 62 in FIG. 4(A) for the reasons discussed in the above passage of Takemura. Accordingly, it is submitted that the low-density source and drain regions on both sides of the channel region that are not identified by reference numeral in FIGS. 4(A)-4(F), one of which is identified by reference numeral 66 in FIG. 7 of Ohtani, are not actually formed entirely under the spacers 68.

Claim 28

It is submitted that Takemura and Ohtani do not disclose or suggest the feature "wherein said low-density source and drain regions having a same conductivity as said high-density source and drain regions are formed at entireties of regions of said semiconductor layer entirely under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers" recited in dependent claim 28 for at least the same reasons discussed above that Takemura and Ohtani do not disclose or suggest the similar feature of claim 22.

Claims 31, 34, 35, and 37

It is submitted that Takemura and Ohtani do not disclose or suggest the feature "[wherein] the source and drain electrodes do not contact the spacers" recited in dependent claims 31, 34, 35, and 37.

As apparently recognized by the Examiner, Takemura does not disclose or suggest this feature of claims 31, 34, 35, and 37 because in FIGS. 5A-5D and 6A-6D of Takemura relied on by the Examiner, the source and drain electrodes 29 and 30 contact the spacers 22. However, the Examiner considers this feature to be taught in FIG. 8(C) of Ohtani, stating as follows with respect to claims 31 and 35 depending from claim 12:

> Re claim 31, Ohtani discloses in fig. 8 source and drain electrodes (14a [*sic*; should be 114a], 114b) that do not contact a capping layer (unnumbered horizontal region covering gates 104 and 105); and wherein the source and drain electrodes do not

> contact the spacers (unnumbered vertical region on the sidewall of gates 104 and 105).
>
> Re claim 35, Ohtani discloses the source and drain electrodes (14a [*sic*], 114b) do not contact the high density source drain regions via any electrode material filling any contact holes; the source and drain electrodes (14a [*sic*], 114b) do not contact the capping layer; and the source and drain electrodes (14a [*sic*], 114b) do not contact the spacers.

The Examiner makes similar statements with respect to claims 34 and 37 depending from claim 22.

However, the Examiner has not clearly articulated any reasons why it would have been obvious for one of ordinary skill in the art to use the source and drain electrodes 114a and 114b in FIG. 8(C) of Ohtani in the thin film transistors in FIGS. 5A-5D and 6A-6D of Takemura as required by MPEP 2143, such that the Examiner has not established a *prima facie* case of obviousness with respect to claims 31 and 34.

Furthermore, it is submitted that column 17, lines 61-67, of Takemura specifically teaches away from the Examiner's apparent proposal to use the source and drain electrodes 114a and 114b in FIG. 8(C) of Ohtani that do not contact the spacers 68 in the thin film transistors in FIGS. 5A-5D and 6A-6D. Specifically, column 17, lines 61-67, of Takemura states as follows in discussing FIGS. 5A-5D of Takemura (emphasis added):

> The NTFT thus, obtained comprises a triangular silicon oxide 22 to establish a contact portion between the source/drain regions and the contact in a so-called self-aligned manner. Moreover, the position of the contact portion can be set irrespective of the shrinking of the glass substrate 11. Furthermore, the contact portion can be set very near to the channel forming region.

See the similar passage in column 18, lines 51-60, discussing FIGS. 6A-6D of Takemura. See also column 25, lines 33-39, of Takemura, which reads as follows (emphasis added):

> As described in the foregoing, the present invention is of great use in fabricating TFTs with improved characteristics and yet, with increased product yield.
>
> In addition to above, the position of the contact in the source/drain regions can be automatically set by providing the insulator in contact with the gate contact in a self aligned manner.

Thus, by forming the contacts 29 and 30 in FIGS. 5D and 6D of Takemura so that they contact the spacers 22, the positions of the contacts 29 and 30 can be automatically set and the contacts 29 and 30 can be formed very near to the channel forming region 18. Accordingly, it is submitted that there would have been no reason for one of ordinary skill in the art to form the contacts 29 and 30 in FIGS. 5D and 6D of Takemura so that they are spaced away from the spacers 22 to obtain the configuration shown in FIG. 8(C) of Ohtani.

Conclusion—Rejections 2 and 3

For at least the foregoing reasons, it is respectfully requested that the rejection of claims 12, 26, 28-31, 35, and 36 (rejection 2) and claims 22, 24, 27, 32-34, 37, and 38 (rejection 3), i.e., claims 12, 28, 31, and 35 discussed above and claims 26, 29, 30, and 36 depending from claim 12, and claims 22, 34, and 37 discussed above and claims 24, 27, 32, 33, and 38 depending from claim 22) under 35 USC 103(a) as being unpatentable over Takemura in view of Ohtani be withdrawn.

Rejection 5

Claim 25 has been rejected under 35 USC 103(a) as being unpatentable over Takemura in view of Yamazaki '648 and Yamazaki et al. '502 (Yamazaki '502) (U.S. Patent Application Publication No. 2003/0207502). This rejection is respectfully traversed.

Notwithstanding the position taken by the Examiner, it is submitted that claim 25 is patentable over Takemura, Yamazaki '648, and Yamazaki '502 at least for the same reasons discussed above that claim 22 from which claim 25 depends is patentable over Takemura and Yamazaki '648.

Accordingly, for at least the foregoing reasons, it is respectfully requested that the rejection of claim 25 under 35 USC 103(a) as being unpatentable over Takemura in view of Yamazaki '648 and Yamazaki '502 be withdrawn.

Conclusion

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

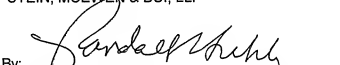
Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this paper, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

STEIN, MCEWEN & BUI, LLP

Date: 05/16/08

By: 

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